REMARKS/ARGUMENTS

1.) Claim Amendments

The Applicant has amended claims 8, 12 and 13. Accordingly, claims 1-14 and 17-19 are pending in the application. Favorable reconsideration of the application is respectfully requested in view of the foregoing amendments and the following remarks.

2.) Allowable Subject Matter

The Applicant gratefully acknowledges the conditional allowance of claims 8, 12 and 13. Claims 8, 12 and 13 have been amended to incorporate their base claims and any intervening claims. Claims 8, 12 and 13 are therefore in condition for allowance.

3.) Examiner Objections - Specification

The Examiner objected to the disclosure due to informalities. The Applicant has amended the specification as suggested by the Examiner. The Examiner's consideration of the amended specification is respectfully requested.

4.) Examiner Objections - Claims

The Examiner objected to Claim 13 due to informalities. The Application has amended the claim to correct the informalities. The Examiner's consideration of the amended claim is respectfully requested.

5.) Claim Rejections – 35 U.S.C. § 103(a)

The Examiner rejected claims 1-5 under 35 U.S.C. § 103(a) as being unpatentable over Eriksson, et al. (US 6,011,815) in view of Sridharan (US 2003/005805). Applicant respectfully traverses the rejection. Examiner admits that Eriksson does not teach a device having a transfer function with at least one zero (see page 5 of the Office Action). According to the Examiner, Sridharan teaches this missing element. However, Sridharan discloses a method to reduce in-band phase noise, introduced by a delta-sigma modulator controlled fractional divider. Although Sridharan discusses zeros in a transfer, these zeros refer to the transfer of the noise (as a function

of frequency) of the control-signal that drives the divider in the feedback path of the Phase Lock Loop (PLL). But these zeros do not appear in the closed-loop transfer of the PLL. These zeros only suppress ("shape") the low-frequency phase jitter generated by the delta-sigma modulators. Note that the output signal of the digital cancellation logic in Figures 3, 5, 6 and 7 drives the integer divider and controls how, in time, the divider will divide between N-1, N or N+1 (for instance) in order to arrive, on average, in a division-factor with a fractional part. But the *average* transfer of the total divider-chain will not have a zero in its transfer. The average transfer of the divider chain, seen in block 13 in Figure 2, is still: "N.F" with N = integer part and F=fractional part and no zero is introduced in this transfer.

In contrast, in the present application a zero is introduced in the feedback-path. This is quite different from the zeros as introduced for the noise shaping of the phase jitter of the control-signal that controls the division-factor of the divider-chain in the feedback path of the PLL. Because Sridharan fails to teach a device having a transfer function with at least one zero, the allowance of claims 1-5 is respectfully requested.

The Examiner rejected claim 6 under 35 U.S.C. § 103(a) as being unpatentable over Eriksson in view of Sridharan, and further in view of Liang, et al. (US 5,550,515). As noted above, neither Eriksson nor Sridharan teach a device having a transfer function with at least one zero. Liang fails to remedy this deficiency. Therefore, the allowance of claim 6 is respectfully requested.

The Examiner rejected claim 7 under 35 U.S.C. § 103(a) as being unpatentable over Eriksson in view of Sridharan in view of Liang, and further in view of Perrett, et al. (US 6,018,275). As noted above, Sridharan does not teach a device having a transfer function with at least one zero. Neither Liang nor Perrett fail to remedy this deficiency. Therefore, the allowance of claim 7 is respectfully requested.

The Examiner rejected claims 9 and 10 under 35 U.S.C. § 103(a) as being unpatentable over Eriksson in view of Sridharan, and in further view of Okumura (US 6,032,277). As noted above, neither Eriksson nor Sridharan teach a device having a transfer function with at least one zero. Okumura fails to remedy this deficiency. Therefore, the allowance of claims 9 and 10 is respectfully requested.

The Examiner rejected claim 11 under 35 U.S.C. § 103(a) as being unpatentable over Eriksson in view of Sridharan, and further in view of Okumura and in further view of Perrett. As noted above, neither Eriksson nor Sridharan teach a device having a transfer function with at least one zero. Okumura and Perrett fail to remedy this deficiency. Therefore, the allowance of claim 11 is respectfully requested.

The Examiner rejected claims 14, 17 and 18 under 35 U.S.C. § 103(a) as being unpatentable over Eriksson in view of Sridharan. As noted above, neither Eriksson nor Sridharan teach a device having a transfer function with at least one zero. Therefore, the allowance of claims 14, 17 and 18 is respectfully requested.

The Examiner rejected claim 19 under 35 U.S.C. § 103(a) as being unpatentable over Eriksson in view of Sridharan, and further in view of Liang. As noted above, neither Eriksson nor Sridharan teach a device having a transfer function with at least one zero. Liang fails to remedy this deficiency. Therefore, the allowance of claim 19 is respectfully requested.

CONCLUSION

In view of the foregoing remarks, the Applicant believes all of the claims currently pending in the Application to be in a condition for allowance. The Applicant, therefore, respectfully requests that the Examiner withdraw all rejections and issue a Notice of Allowance for all pending claims.

The Applicant requests a telephonic interview if the Examiner has any questions or requires any additional information that would further or expedite the prosecution of the Application.

Respectfully submitted,

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